

## CLAIMS

1: A print engine/controller chip configurable to be coupled with others to drive a multi-segment printhead comprising:

5 a memory buffer for receiving compressed page data;

image decoders to perform an expansion, in pipeline fashion, of the compressed page data;

a half-toner/compositer to composite respective strips of the decoded image planes; and

a printhead interface to output the composite strip to a printhead

the printhead interface including:

10 two LineSyncGen units, a first LineSyncGen unit providing a synchronization signal for multiple print engine/controller chips and a second LineSyncGen unit adapted to pulse a paper drive stepping motor.

2. The print engine/controller of claim 1 wherein:

15 each LineSyncGen unit produces an external signal to enable line synchronization, a generation in each LineSyncGen unit producing a pulse in a number of cycles until instructed to stop, the pulse defining a start of a next line.

3. The print engine/controller of claim 2 wherein:

20 number of cycles is determined by a register, each cycle being long enough to allow a line to print and another line to load.

4. The print engine/controller of claim 1 further comprising:

25 an output interface for transferring data to a printhead and enabling feedback from a specific segment.

5. The print engine/controller of claim 4 wherein:

the output interface contains a state machine that follows a printhead loading order and a dot count for each color.

6. The print engine/controller of claim 4 wherein:  
the output interface is directly connected to a line loader/format unit and the printhead.
7. The print engine/controller of claim 4 wherein:  
5 the output interface loads data into the printhead from a first data source which is all binary ones causing a firing of all nozzles of the printhead during a subsequent print cycle; and  
the output interface loads data into the printhead from a second data source being an input held in a transfer register of a line loader/format unit.
- 10 8. The print engine/controller of claim 4 wherein:  
the output interface has a number of connections to the printhead, comprising a number of color connections clocked into a second number of segments per transfer to one or two segment groups.
- 15 9. The print engine/controller of claim 4 wherein:  
the output interface maintains a count of the number of dots of each color fired from the printhead, the count being a value which is independently cleared under processor control.
10. The print engine/controller of claim 9 wherein:  
20 a dot count is used by a processor on the chip to update a QA chip in order to predict when an ink cartridge runs out of ink.
11. The print engine/controller of claim 10 wherein:  
the processor communicated with the output interface via a register set that allows the processor to  
25 parameterize a print as well as receive feedback about a print.
12. The print engine/controller of claim 10 wherein;  
an updated drop count is written to the QA chip after a page is completed.
- 30 13. The print engine/controller of claim 1 wherein:

the pipeline fashion expansion further comprises the expansion, in parallel with the layers, of a Group 4 Fax-compressed bi-level dither matrix selection map.

14. The print engine/controller of claim 13 wherein:

5 the pipeline fashion expansion further comprises a second stage dithering of the contone CMYK layer using a dither matrix selected by the dither matrix select map.

15. The print engine/controller of claim 1, wherein:

10 the half-toner/compositor further comprises a number of scale units, each scale unit receiving data from a buffer layer and at least one scale unit receiving two control bits, the control bits being an advance dot bit and an advance line bit.

16. The print engine/controller of claim 15, wherein:

15 the advance dot bit allows for the generation of multiple instances of identical dot data and the advance line bit provides for truncation of data according to a printer margin.

17. The print engine/controller of claim 15, wherein:

the buffer layers comprise contone layers, a bi-level spot1 layer and a dither select matrix layer, each of which may be scaled independently.

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